IN THE CLAIMS:

Please cancel claims 1-10 and 19-27 without prejudice or disclaimer. All pending claims and their present status are produced below.

1-10. (Cancelled)

11. (Previously Presented) An embedded processor for providing connectivity in a communications system, comprising:

a 32-bit arithmetic-logic unit (ALU) comprising a first input, a second input, and an output, the ALU for performing an operation on a first 32-bit operand and a second 32-bit operand and for producing a 32-bit result, the operation specified in a 32-bit instruction fetched by the ALU;

a 32-bit register file for temporarily holding data, the 32-bit register file coupled to the first input of the ALU and communicatively coupled to the second input of the ALU for providing the first and the second 32-bit operand and coupled to the output of the ALU to receive the 32-bit result as an output from the ALU;

a memory device communicatively coupled with the second input of the ALU for providing the ALU input-data and communicatively coupled to the output of the ALU for receiving result-data, the memory device comprising a storage location of a size of less than 32 bits;

a sign extender coupled to the memory device for expanding the input-data from the memory to 32-bit data; and

a multiplexer comprising a first and a second input and an output, the first input coupled to the sign extender for receiving the expanded 32-bit data, the second input

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coupled to the 32-bit register, and the output coupled to the ALU, the multiplexer

for selecting between the inputs the source for providing the first 32-bit operand

to the ALU.

12.   (Previously Presented) The embedded processor of claim 11, further comprising:

a truncator communicatively coupled to the ALU and the memory device, the truncator

for converting the 32-bit result received from the ALU to a data unit of the size of

the storage location in the memory device.

13.   (Previously Presented) The embedded processor of claim 11, wherein the multiplexer

further comprises a third input communicatively coupled to an immediate.

14.   (Previously Presented) The embedded processor of claim 13, wherein the immediate is

less than 32 bits and wherein the immediate is coupled to the sign expander for converting the

immediate to an expanded 32-bit immediate, the sign expander further coupled to the third input

of the multiplexer for communicating the expanded 32-bit immediate.

15.   (Previously Presented) The embedded processor of claim 13, wherein the 32-bit

instruction comprises a 5-bit OpCode for specifying the operation, an 11-bit source address for

specifying a first source location for the first 32-bit operand, a 5-bit source address for specifying

a second source location for the second 32-bit operand, and an 11-bit destination address for

specifying a destination location to store the 32-bit result.

16.   (Previously Presented) The embedded processor of claim 15, wherein the immediate

comprises a 4-bit immediate and a 7-bit immediate, the embedded processor further comprising:

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a general register file having no more than 32 data registers, the general register file

comprising memory addressing information;

a second multiplexer comprising a first, a second, and a third input and an output, the first

input coupled to the 7-bit immediate, the second input coupled to the 4-bit

immediate, and the third input coupled to the general register file, the multiplexer

for selecting between the inputs to provide an output;

an address register file having no more than 8 registers, the address register file

comprising addressing information and an output;

an adder coupled to the output of the second multiplexer for receiving one of the 7-bit

immediate, the 4-bit immediate, and the general register file, and the adder

coupled to the address register for adding the output of the second multiplexer

with the output of the address register and for providing a sum; and

a third multiplexer comprising a first input, a second input, and an output, the first input

coupled to the address register file, the second input coupled to the adder for

receiving the sum, the third multiplexer for choosing between the address register

file output and the sum thereby providing the 11-bit source address of the 32-bit

instruction according to an address mode.

17.   (Previously Presented) The embedded processor of claim 16, wherein the address mode

is one of the group consisting of a Register + Immediate, a Register + Register Indirect, a

Register + Immediate Auto-Increment, a Register Direct, and an Immediate addressing mode.

18.   (Previously Presented) The embedded processor of claim 11, wherein the 32-bit

instruction comprises a 5-bit OpCode for specifying the operation, an 11-bit source address for

specifying a first source location for the first 32-bit operand, a 5-bit source address for specifying

a second source location for the second 32-bit operand, and an 11-bit destination address for

specifying a destination location to store the 32-bit result.

19-27. (Cancelled)

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